

Ayatallah Elakhras

Computer Science Ph.D. Candidate

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🎓 Education

2020 – 2026	Ph.D. in Computer and Communication Sciences	EPFL, Switzerland
	Thesis: Efficient Data Steering in Dataflow Circuits. Advisors: Prof. Paolo Ienne and Prof. Lana Josipović. Research Interests: Dataflow Architecture , Specialized Computing , Compilers , Heterogeneous Systems .	
2015 – 2020	B.Sc. in Computer Engineering	American University in Cairo, Egypt
	Thesis: FPGA-Based Accelerator for a Truck Detection Algorithm.	GPA: 3.96/4.0

🏆 Honors and Awards

2026	Best Paper Honorable Mention at ASPLOS'26.
2026	Best Paper Award Runner-up at FPGA'26.
2024	Google PhD Fellowship for exceptional PhD research in Distributed Systems and Parallel Computing.
2022	Best Paper Award Nominee at FPL'22.
2020	EDIC Fellowship , IC school, EPFL, for new PhD students with an exceptional academic record.
2020	Summa cum laude , B.Sc. degree, American University in Cairo.
2018, 2019	Outstanding Academic Achievers' Honors Assembly , American University in Cairo.

💼 Work Experience

Sep 2020 – Aug 2026	Researcher and Ph.D. Candidate	EPFL, Switzerland
	Compiler optimization, MLIR infrastructure, performance engineering, and transformation verification	
	- Developed MLIR compiler passes that lower sequential C/C++ control flow into parallel dataflow representations, reducing the resulting execution time by up to 75%. - Designed and implemented optimization transformations for parallel execution, memory access coordination, tagging, and out-of-order execution. - Built graph-rewriting passes for dataflow IRs and validated their correctness using model checking. - Analyzed performance across workloads, identifying execution, memory, and communication bottlenecks. - Collaborated with researchers across EPFL and ETH Zurich on compiler transformations, verification methodology, and architecture-aware optimization. - Mentored student contributors implementing and evaluating MLIR compiler passes.	
Oct 2023 – Mar 2024	Research and Advanced Development Intern	AMD, CO, USA
	Industrial R&D in heterogeneous computing and AI workload mapping	
	- Extended an architecture-aware scheduling and design-space exploration framework for mapping deep-neural-network workloads onto AMD AI Engines. - Modeled compute resources, interconnect constraints, communication patterns, and spatial-placement decisions to support compiler-guided workload mapping. - Evaluated mapping strategies on AI workloads and characterized performance-relevant spatial patterns. - Collaborated with industrial researchers to translate architecture constraints into mapping abstractions.	
Jun 2020 – Sep 2020	Undergraduate Research Intern	EPFL, Switzerland
	Accelerated and deployed a Backprojection SPIRAL kernel on an AWS FPGA instance using Vitis HLS.	

- Profiled runtime across input sizes to identify bottlenecks and improve throughput through loop unrolling.
- Exported the kernel as a Vivado IP and evaluated its integration with multiple memory configurations.

Jun 2019 – Aug 2019 **Machine Learning Intern**

AvidBeam Technologies, Egypt

- Developed a deep learning model using multi-attribute learning for pedestrian attribute recognition.

Aug 2017 – Sep 2017 **Embedded Systems Intern**

Mentor Graphics, Egypt

- Built an embedded system connecting Samsung ARTIK 030 to temperature sensors through i2c bus.

Publications

- 2026 Yann Herklotz, [Ayatallah Elakhras](#), Martina Camaioni, Paolo lenne, Lana Josipović, and Thomas Bourgeat. **Graphiti: Formally Verified Out-of-Order Execution in Dataflow Circuits. [ASPLOS'26](#). Best Paper Honorable Mention.**
- 2026 Rouzbeh Piryadi, [Ayatallah Elakhras](#), Mirjana Stojilović, and Paolo lenne. **Out with LSQs: Custom Circuits for Memory Access Reordering in Dynamic HLS. [FPGA'26](#). Best Paper Award Runner-up.**
- 2025 [Ayatallah Elakhras*](#), Jiahui Xu*, Martin Erhart, Paolo lenne, and Lana Josipović. **ElasticMiter: Formally Verified Dataflow Circuit Rewrites. [ASPLOS'25](#). *Equal contribution [\[pdf\]](#)[\[DOI\]](#).**
- 2024 [Ayatallah Elakhras](#), Andrea Guerrieri, Lana Josipović, and Paolo lenne. **Survival of the Fastest: Enabling More Out-of-Order Execution in Dataflow Circuits. [FPGA'24](#) [\[pdf\]](#)[\[DOI\]](#).**
- 2023 [Ayatallah Elakhras](#), Riya Sawhney, Andrea Guerrieri, Lana Josipović, and Paolo lenne. **Straight to the Queue: Fast Load-Store Queue Allocation in Dataflow Circuits. [FPGA'23](#) [\[pdf\]](#)[\[DOI\]](#)[\[video\]](#).**
- 2022 [Ayatallah Elakhras](#), Andrea Guerrieri, Lana Josipović, and Paolo lenne. **Unleashing Parallelism in Elastic Circuits with Faster Token Delivery. [FPL'22](#). Best Paper Award Nominee [\[pdf\]](#)[\[DOI\]](#).**

Invited Talks

Feb 2026	Google, Sunnyvale	Custom Dataflow Circuits for Memory Access Reordering
Oct 2025	American University in Cairo	Dynamically Scheduled High-Level Synthesis
Aug 2025	Synopsis Visit to EPFL	Challenges in Reasoning about Dataflow Circuits
Apr 2025	ASPLOS'25 (conference talk)	ElasticMiter: Formally Verified Dataflow Circuit Rewrites
Apr 2024	AMD (end-of-internship talk)	Design Space Exploration for AI Engines
Mar 2024	FPGA'24 (conference talk)	Survival of the Fastest: Enabling More Out-of-Order Execution
Feb 2023	FPGA'23 (conference talk)	Straight to the Queue: Fast Load-Store Queue Allocation
Sep 2022	FPL'22 (conference talk)	Unleashing Parallelism in Elastic Circuits with Faster Token Delivery

Teaching and Mentoring

Project Supervision at EPFL

- 2025 – present Yuan Qin [M.Sc. Thesis](#)
- Optimizing dataflow circuits by globally analyzing multiple producer-consumer relationships and generating optimal Mux trees to implement complicated control flow decisions.
- 2025 – present Zeinab Pourghesari [Three-Month Internship](#)
- Enhanced our Gated-Single Assignment MLIR library to support loops with multiple loop exits.
- 2024 – 2025 Giacomo Sansone [M.Sc. Thesis](#)
- Conducted empirical research on where out-of-order execution is advantageous in dataflow circuits and implemented our fast token delivery strategy in MLIR.
- 2024 – 2025 Dana Kossaybati [Six-Month Internship](#)

- Automated the generation of tagged components and implemented an MLIR pass for introducing out-of-order execution in dataflow circuits.
- 2024 Anushka Allawadi [One-Month Internship](#)
- Implemented a pattern match rewriter in MLIR for optimizing dataflow circuits.
- 2023 Teodor Cvijović [Two-Month Internship](#)
- Implemented a control dependence analysis pass in MLIR.
- 2023 Ahmed Salem [Three-Month Internship](#)
- Experimented a VHDL library of tagged dataflow circuit components.
- 2023 Gianluca Radi [Semester Project](#)
- Implemented loop disordering in dataflow circuits and extended the interface of the produced circuits to support multithreading.
- 2022 Riya Sawhney [Two-Month Internship](#)
- Researched a load-store queue interface to exploit parallelism in dataflow circuits.

Teaching Assistance at EPFL

2021 – 2025 Computer Architecture I and II

- Guided 200+ Bachelor's students through lab sessions in VHDL, Verilog, NIOS II, and RISC-V assembly, and co-designed midterm and final exams.

Teaching Assistance at the American University in Cairo

2018 Computer Organization and Assembly Language Programming

- Presented tutorials to introduce Bachelor's students to MIPS assembly.

Selected Open-Source Projects

Fast Token Delivery	MLIR conversion pass from the control flow (cf) dialect to the handshake dialect implementing my proposed dataflow circuit generation strategy . Student Contributors: Yuan Qin, Giacomo Sansone, Dana Kossaybati.
Straight to the Queue	MLIR handshake transformation pass implementing an efficient load-store queue interface . Student Contributors: Giacomo Sansone, Zeinab Pourghesari.
Fine-Grained Disorder	MLIR transformation pass introducing fine-grained tagging and out-of-order execution . Student Contributor: Dana Kossaybati.

Professional Service

[Doctoral Admission Prefiltering Committee, EPFL](#): Evaluated doctoral applicants for EPFL's PhD program.

[PhD Application Mentor, EPFL](#): Supported prospective PhD applicants by reviewing application materials.

[Primary Reviewer](#)

- ACM Transactions on Design Automation of Electronic Systems (TODAES).
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

[Secondary Reviewer](#)

- ACM/IEEE International Conference on Computer-Aided Design (ICCAD).
- ACM International Symposium on Field-Programmable Gate Arrays (FPGA).
- IEEE International Conference on Field-Programmable Logic and Applications (FPL).
- IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM).

Languages

[Arabic](#) (native), [English](#) (proficient), [French](#) (beginner)
